What is claimed is:

1. A semiconductor integrated circuit device comprising:

a memory cell having first and second transfer MISFETs, first and second drive MISFETs and first and second load MISFETs, each disposed at an intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-coupled with the second drive MISFET and second load MISFET,

wherein the first and second transfer MISFETs and the first and second drive MISFETs are formed over the main surface of a semiconductor substrate,

wherein a first insulating film is formed over the semiconductor substrate and a first opening is formed in the first insulating film,

wherein a first capacitor element is formed over the sidewall and bottom of the first opening, the first capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the first opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film,

wherein a supply voltage line electrically connected to the first and second drive MISFETs and a reference

voltage line electrically connected to the first and second drive MISFETs are formed over the first capacitor element,

wherein the lower electrode forms a first storage node of the memory cell by electrically connecting a drain of the first drive MISFET, a drain of the first load MISFET, a gate electrode of the second drive MISFET and a gate electrode of the second load MISFET, and a second storage node of the memory cell by electrically connecting a drain of the second drive MISFET, a drain of the second load MISFET, a gate electrode of the first drive MISFET and a gate electrode of the first load MISFET, and

wherein the first capacitor element is electrically connected between the first storage node and second storage node, and the supply voltage line, between the first storage node and second storage node, and the reference voltage line, or between the first storage node and the second storage node.

2. A semiconductor integrated circuit device according to Claim 1, wherein the first opening reaches the gate electrode of the first and second drive MISFETs and the drain of the first and second load MISFETs.

3. A semiconductor integrated circuit device according to Claim 1, wherein the second conductive film extends over the first insulating film and is connected, over the first insulating film, to a conductive layer

formed above the second conductive film

4. A semiconductor integrated circuit device according to Claim 1, wherein the first and second load MISFETs are formed above the first and second transfer MISFETs and the first and second drive MISFETs, the first load MISFET has a source, a channel region and a drain formed in a first laminate extending in a direction perpendicular to the main surface of the semiconductor substrate and a gate electrode formed over the sidewall of the first laminate via a gate insulating film, the second load MISFET has a source, a channel region and a drain formed in a second laminate extending in a direction perpendicular to the main surface of the semiconductor substrate and a gate electrode formed over the sidewall of the second laminate via a gate insulating film, and the first insulating film is formed to cover the first and second load MISFETs.

5. A semiconductor integrated circuit device according to Claim 1, wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate, a power supply circuit is formed in a second region over the main surface of the semiconductor substrate,

wherein in a second opening formed in the first insulating film in the second region, a second capacitor element having the first conductive film formed along the

sidewall and bottom of the second opening as a lower electrode, the second insulating film formed over the first conductive film as an insulator and the second conductive film formed over the second insulating film as an upper electrode is formed,

wherein the power supply circuit feeds the memory cell an operating voltage, and

wherein the second capacitor element is electrically connected between the operating voltage and ground potential.

6. A semiconductor integrated circuit device according to Claim 5, wherein the bottom of at least one of the first opening and the second opening reaches a third insulating film formed below the first insulating film, and the first and second conductive films each extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the first insulating film.

7. A semiconductor integrated circuit device comprising:

a memory cell having first and second transfer MISFETs, first and second drive MISFETs and first, and second load MISFETs, each disposed at an intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-

coupled with the second drive MISFET and second load MISFET; and

a power supply circuit,

wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate and the power supply circuit is formed in a second region over the main surface of the semiconductor substrate,

wherein a first insulating film is formed over the semiconductor substrate,

wherein in a second opening formed in the first insulating film in the second region, a second capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the second opening, as an insulator, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film, and

wherein the power supply circuit feeds the memory cell with an operating voltage and the second capacitor element is electrically connected between the operating voltage and ground voltage.

8. A semiconductor integrated circuit device according to claim 7, wherein the bottom of the second opening reaches a third insulating film formed below the first insulating film, and the first conductive film and

the second conductive film each extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the first insulating film.

9. A semiconductor integrated circuit device, comprising a first insulating film formed over a semiconductor substrate, a second opening formed in the first insulating film, and a capacitor element having, as a lower electrode, a first conductive film formed along the sidewall and bottom of the second opening, as a capacitor insulator film, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film formed over the sidewall and the bottom of the second opening, said capacitor element constituting an analog circuit.

10. A semiconductor integrated circuit device according to Claim 9, wherein the bottom of the first opening reaches a third insulating film formed below the first insulating film, and the first conductive film and second conductive film each extends over the first insulating film and is connected, over the first insulating film, to a conductive layer formed above the first insulating film.

11. A manufacturing method of a semiconductor

integrated circuit device, comprising:

a memory cell having first and second transfer MISFETs, first and second drive MISFETs and first and second load MISFETs, each disposed at the intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-coupled with the second drive MISFET and second load MISFET,

the method comprising the steps of:

(a) forming the first and second transfer MISFETs and the first and second drive MISFETs over the main surface of a semiconductor substrate;

(b) forming a first insulating film over the semiconductor substrate and making a first opening in the first insulating film;

(c) forming a first conductive film over the sidewall and bottom of the first opening, forming a first storage node of the memory cell by electrically connecting, via the first conductive film, a drain of the first drive MISFET, a drain of the first load MISFET, a gate electrode of the second drive MISFET and a gate electrode of the second load MISFET, and forming a second storage node by electrically connecting, via the first conductive film, a drain of the second drive MISFET, a drain of the second load MISFET, a gate electrode of the first drive MISFET and a gate electrode of the first load MISFET;

(d) forming a second insulating film over the first conductive film, forming a second conductive film over the second insulating film, and forming a first capacitor element having the first conductive film as a lower electrode, the second insulating film as a capacitor insulator film and the second conductive film as an upper electrode; and

(e) forming a supply voltage line and a reference voltage line over the first capacitor element, said first capacitor element being electrically connected between the first storage node and second storage node, and the supply voltage line, between the first storage node and second storage node, and the reference voltage line, or between the first storage node and the second storage node.

12. A manufacturing method of a semiconductor integrated circuit device according to Claim 11, wherein the step (b) further comprises the steps of:

(b1) forming a third opening in the first insulating film;

(b2) depositing a third conductive film over the first insulating film including the inside of the third opening to fill the third conductive film in the second opening; and

(b3) removing the third conductive film outside the third opening to leave the third conductive film in the

third opening,

said steps (b1) to (b3) being carried out prior to the formation of the first opening.

13. A manufacturing method of a semiconductor integrated circuit device according to Claim 11, wherein the first opening is formed so as to reach the gate electrode of the first and second drive MISFETs and the drain of the first and second load MISFETs.

14. A manufacturing method of a semiconductor integrated circuit device according to Claim 11, wherein the step (d) comprises the steps of:

(d1) patterning the second conductive film to extend over the first insulating film;

(d2) forming a fourth insulating film over the first insulating film;

(d3) forming the fourth insulating film to form a connecting hole reaching the second conductive film which extends over the first insulating film; and

(d4) forming a conductive layer in the connecting hole.

15. A manufacturing method of a semiconductor integrated circuit device according to Claim 11,

wherein the first load MISFET has a source, a channel region and a drain formed in a first laminate extending in a direction perpendicular to the main surface of the

semiconductor substrate and a gate electrode formed over the sidewall of the first laminate via a gate insulating film,

wherein the second load MISFET has a source, a channel region and a drain formed in a second laminate extending in a direction perpendicular to the main surface of the semiconductor substrate and a gate electrode formed over the sidewall of the second laminate via the gate insulating film,

the method further comprising:

(f) over the first and second transfer MISFETs and first and second drive MISFETs, forming a first intermediate conductive layer for electrically connecting the gate electrode of the second drive MISFET to the drain of the first drive MISFET and forming a second intermediate conductive layer for electrically connecting the gate electrode of the first drive MISFET to the drain of the second drive MISFET;

(g) forming, via an insulating film, first and second gate extraction electrodes over the first and second intermediate conductive layers;

(h) after the step (g), forming the first and second laminates above the first and second gate extraction electrodes to electrically connect the drain of the first vertical MISFET formed in the first laminate to the first

intermediate conductive layer and the drain of the second vertical MISFET formed in the second laminate to the second intermediate conductive layer;

(i) electrically connecting the gate electrode of the first load MISFET formed, via the first gate insulating film, over the sidewall of the first laminate to the first gate extraction electrode and connecting the gate electrode of the second vertical MISFET formed, via the gate insulating film, over the sidewall of the second laminate to the second gate extraction electrode;

(j) electrically connecting the gate electrode of the first vertical MISFET formed, via the gate insulating film, over the sidewall of the first laminate to the first gate extraction electrode, and electrically connecting the gate electrode of the second vertical MISFET formed, via the gate insulating film, over the sidewall of the second laminate to the second gate extraction electrode;

(k) over the first gate extraction electrode, forming the first opening so as to bring the first gate extraction electrode into contact with the second intermediate conductive layer and forming another first opening so as to bring the second gate extraction electrode into contact with the first intermediate conductive layer; and

(l) forming the first conductive film over the sidewall and bottom of the first opening, and electrically

connecting, via the first conductive film, the first gate extraction electrode to the second intermediate conductive layer, and electrically connecting, via the first conductive film, the second gate extraction electrode to the first intermediate conductive layer.

16. A manufacturing method of a semiconductor integrated circuit device according to Claim 11, wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate, a power supply circuit for feeding the memory cell with an operating voltage is formed in a second region over the main surface of the semiconductor substrate,

the method further comprising the steps of:

(f) forming a second opening in the first insulating film in the second region; and

(g) forming the first conductive film along the sidewall and bottom of the second opening, forming the second insulating film over the first conductive film in the second opening, forming the second conductive film over the second insulating film in the second opening, and forming a second capacitor element which has the first conductive film as a lower electrode, the second insulating film as a capacitor insulator film and the second conductive film as an upper electrode and is electrically connected between the power supply circuit and memory cell,

and a ground potential.

17. A manufacturing method of a semiconductor integrated circuit device comprising:

a memory cell having first and second transfer MISFETs, first and second drive MISFETs and first and second load MISFETs, each disposed at an intersection between a pair of complementary data lines and a word line, the first drive MISFET and first load MISFET being cross-coupled with the second drive MISFET and second load MISFET; and

a power supply circuit for feeding the memory cell with an operating voltage,

wherein the memory cell is formed in a first region over the main surface of the semiconductor substrate and the power supply circuit is formed in a second region over the main surface of the semiconductor substrate,

the method comprising the steps of:

(a) forming a first insulating film over the semiconductor substrate;

(b) making a second opening in the first insulating film in the second region; and

(c) forming a first conductive film over the sidewall and bottom of the second opening, a second insulating film over the first conductive film, a second conductive film over the second insulating film, and a second capacitor

element which has the first conductive film as a lower electrode, the second insulating film as a capacitor insulator film and the second conductive film as an upper electrode and is electrically connected between the operating voltage and ground potential.

18. A manufacturing method of a semiconductor integrated circuit device according to Claim 17, wherein the step (b) further comprises the steps of:

(b1) forming a third opening in the first insulating film;

(b2) depositing a third conductive film over the first insulating film inside of the third opening to fill therein the third conductive film; and

(b3) removing the third conductive film outside the third opening to leave the third conductive film in the third opening,

said steps (b1) to (b3) being carried out prior to the formation of the second opening.

19. A manufacturing method of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first insulating film over a semiconductor substrate;

(b) forming a second opening in the first insulating film; and

(c) forming a first conductive film along the

sidewall and bottom of the second opening, a second insulating film over the first conductive film, a second conductive film over the second insulating film and a capacitor element having the first conductive film as a lower electrode, the second insulating film as an insulator and the second conductive film as an upper electrode,

wherein an analog circuit is formed using the capacitor element.

20. A manufacturing method of a semiconductor integrated circuit device according to Claim 19, further comprising the steps of:

(b1) forming a third opening in the first insulating film;

(b2) depositing a third conductive film over the first insulating film including the inside of the third opening to fill therein the third conductive film; and

(b3) removing the third conductive film outside the third opening to leave the third conductive film in the third opening,

wherein said steps (b1) to (b3) are carried out prior to the formation of the second opening.

21. A semiconductor integrated circuit device comprising:

a first insulating film formed over a semiconductor substrate; and

a plurality of second openings formed in the first insulating film,

wherein a capacitor element is formed over the sidewall and bottom of the plurality of second openings and has, as a lower electrode, a first conductive film formed along the sidewall and bottom of the second openings, as an insulator, a second insulating film formed over the first conductive film, and as an upper electrode, a second conductive film formed over the second insulating film in the plurality of second openings.

22. A semiconductor integrated circuit device according to Claim 21, wherein a plurality of interconnect grooves are formed in the first insulating film and an interconnect is formed in the interconnect grooves.